Docket No.: WMP-IFT-679

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Before the Board of Patent Appeals and Interferences

Applic. No.	:	10/662,793	Confirmation No.: 9506
Inventor	:	Alfred Hesener	
Filed	:	September 15, 2003	
Title	:	Control Transducer and Method for Controlling a Switch in a Control Transducer	
TC/A.U.	:	2838	
Examiner	:	Shawn Riley	
Customer No.	:	24131	

AMENDED

BRIEF ON APPEAL

This is an appeal from the final rejection in the Office action dated February 5, 2007, finally rejecting claims 15-28.

Appellants submit this *Brief on Appeal* in triplicate, including payment in the amount of $500.00 to cover the fee for filing the *Brief on Appeal*.

Real Party in Interest:

This application is assigned to Infineon Technologies AG of München, Germany. The assignment will be submitted for recordation upon the termination of this appeal.

Related Appeals and Interferences:

No related appeals or interference proceedings are currently pending which would directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

Status of Claims:

Claims 15-28 are finally rejected and are under appeal. Claims 1-14 were canceled.

Status of Amendments:

No claims were amended after the final Office action.

Summary of Claimed Subject Matter:

Independent device claim 15 recites a switching converter and independent claim 25 recites a method of driving a switch in such a switching converter. Figs. 1 and 7 illustrate exemplary embodiments of the device. Claim 15 relates to the description as follows (the parenthetical expressions referring to the drawings):

a switch (T1 - Fig. 1; T2 - Fig. 7) *including a control terminal* (G), *a first load terminal and a second load terminal* (D, S) - p. 7, line 25, to p. 8, line 3; p. 16, lines 1 - 5;

a rectifier configuration (GL1 - Fig. 1; GL2 - Fig. 7) *connected to said switch* (T1; T2), *said rectifier configuration* (GL1, GL2) *including a plurality of output terminals* (AK1, AK2) *for providing an output voltage* (Uout) *to a load* (RL) - p. 8, lines 11 - 14;

a controller configuration (RA1, RA2) *for providing a control signal* (RS, DRS) *dependent on the output voltage* (Uout) - p. 9, lines 17 - 21; *and*

a drive circuit (AS1; AS2) *for generating drive pulses - p. 9, line 23, to p. 10, line 2 - said drive circuit comparing the control signal* (RS; DRS) *with a reference signal* (Vref; REF2) *in periodical time periods, and, in dependence on the comparison, providing a drive pulse of a given duration or no drive pulse - p. 10, lines 11 - 24*;

said drive pulses turning said switch on and off - p. 10, lines 11- 24.

Independent claim 25 is a method claim. There, the novel method of driving a switch in a switching converter is defined. The method comprises to following steps:

generating a control signal dependent on an output voltage provided by the rectifier configuration – the rectifier provides an output voltage Uout, which forms the basis for the control signal RS for driving the switch. Page 8, lines 21-28.

comparing the control signal with a reference signal in periodical time periods to form a comparison result – page 10, line 11, et seq.

generating a drive signal with drive pulses and, depending on the comparison result, providing a drive pulse of a given duration or no drive pulse – page 10, lines 17-24.

Appellants described an exemplary embodiment of the switching converter according to the invention with reference to Fig. 1 starting on page 7, line 22, of the specification. The switching converter provides an approximately load-independent output voltage Uout from an input voltage Uin. It includes a switch T1, which is designed as a power transistor and is connected, in series with a primary coil L1 of a transformer TR, to an input voltage Uin between a terminal for supply potential and a terminal for reference-ground potential M. The primary coil L1 is inductively coupled to a secondary coil L2, a rectifier, which comprises a series circuit of a diode D1 and a capacitor C1 in the exemplary embodiment, being connected downstream of the secondary coil L2. An output voltage Uout can be tapped off at output terminals AK1, AK2 at the capacitor C1. A load RL, represented as a nonreactive resistor in the exemplary embodiment, can be connected to the output terminals AK1, AK2. The arrangement with the transformer TR, and the rectifier, generally forms a rectifier arrangement GL1 which is connected, in series with the power transistor T1, to the supply voltage Uin.

Appellants outlined on page 8 of the specification, line 17, that when the power transistor T1 is in the on state, the primary coil L1 takes up energy and subsequently outputs it, when the power transistor T1 is in the off state, to the load RL via the secondary coil L2 and the rectifier D1, C1.

It is further stated on page 8 of the specification, line 21, that in order to drive the power transistor T1 a drive circuit AS1 is provided, which generates drive pulses AI according to a control signal RS. The power transistor T1 turns on according to the

drive pulses AI, these drive pulses being fed directly to the gate terminal G of the power transistor T1 in the exemplary embodiment in accordance with figure 1.

As set forth on page 9 of the specification, line 1, the control signal RS is generated by a controller RA1 in dependence on the output voltage Uout. For this purpose, an output voltage signal US is fed to the controller RA1. In order to provide this output voltage signal US, provision is made of an optocoupler OK with a light-emitting diode and a phototransistor PT. The light-emitting diode LED is connected in series with a resistor R1 between the output terminals AK1, AK2 of the rectifier arrangement GL1. The collector-emitter path of the phototransistor PT is connected in series with a resistor R2 between a supply potential V2 and reference-ground potential M. The output voltage signal US, proportional to the output voltage Uout, represents a voltage with respect to reference-ground potential M which can be tapped off at the collector of the phototransistor PT.

With reference to page 10 of the specification, starting at line 11, the comparator arrangement K1 compares the control signal RS with the reference voltage signal Vref at periodic time intervals, prescribed by rising edges of the clock signal CLK in the example. In this case, if the control signal RS is greater than the reference voltage signal Vref, as is the case between the instants t0 and t1 and the instants t2 and t3, then the comparator arrangement generates a drive pulse with each rising edge of a clock pulse at which the control signal RS is greater than the reference signal Vref, the duration of the drive pulses AI corresponding to the duration of the clock pulses of the clock signal CLK in the exemplary embodiment. If the control

signal RS is less than the reference signal Vref, then no drive pulses are generated, as is illustrated within a period of time between the instants t1 and t2.

Appellants outlined in the first paragraph on page 11 of the specification, that Fig. 3 shows an exemplary embodiment of a circuitry realization of a clocked comparator arrangement K1 in accordance with Fig. 1. In this case a comparator K1 is provided, whose noninverting input is fed the control signal and whose inverting input is fed the reference signal Vref. An output signal of the comparator K is fed to a set input S of an RS flip-flop FF, which is driven in clocked fashion by the clock signal CLK. For this purpose, the clock signal CLK is fed to a clock input of the RS flip-flop FF. In this case, the RS flip-flop is designed in such a way that it accepts the signal present at its set input S in each case with a rising edge of the clock signal CLK. If the output signal of the comparator K has an upper level because the control signal RS is greater than the reference signal Vref, then the flip-flop FF is set with a rising edge of the clock signal CLK and a signal with an upper drive level is available at the output Q of the flip-flop. A reset input R of the flip-flop FF is fed a clock signal delayed by means of a delay element D, the flip-flop FF being reset after a delay time prescribed by the delay element D has elapsed after a rising edge of the clock signal CLK. In this case, the delay element D determines the duration of a generated drive pulse, a drive circuit in accordance with figure 3 being able to generate drive pulses which - unlike the illustration in figure 2 - may be shorter or longer than half period durations of the clock signal CLK.

Grounds of Rejection to be Reviewed on Appeal

1. Whether or not claims 15-28 are anticipated by U.S. Patent No. 5,905,370 to Bryson (hereinafter "Bryson") under 35 U.S.C. § 102(b).

Argument:

The underlying law is clear: Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Sys., Inc., 730 F.2d 1440, 221 USPQ 385 (Fed. Cir. 1984). W.L. Gore and Assoc., Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303 (Fed. Cir. 1983).

Appellants respectfully submit that Bryson cannot anticipate the claimed invention because the prior art reference lacks at least one essential element recited in each of the independent claims 15 and 25. We rely on the recitation in claim 15, according to which "the drive circuit [compares] the control signal with a reference signal in periodical time periods, and, in dependence on the comparison, [provides] a drive pulse of a given duration or no drive pulse." Similarly, claim 25 defines a method step of "generating a drive signal with drive pulses and, depending on the comparison result, providing a drive pulse of a given duration or no drive pulse."

In finally rejecting claim 15, the Primary Examiner alleged that Bryson disclose: "said drive circuit comparing . . . the control signal with a reference signal . . . and, in dependence on the comparison, providing a drive pulse . . . of a given duration or no drive pulse." Final rejection, page 3. Respectfully, this is patently wrong.

Bryson does not disclose a switching converter in which a drive pulse of a given duration or no drive pulse is generated in dependence on a comparison between a control signal and a reference signal.

In order to properly understand this statement, we must briefly review the technological foundation underlying the prior art reference. Bryson describes a switching converter which is either driven in PWM (pulse width modulation) mode or in PFM (pulse frequency modulation, pulse skipping mode) depending on the load requirement. While Bryson does not detail the functionality of the converter in its PWM mode operation, it is well know to those of skill in the art that a switching converter with fixed clock generates drive pulses in periodic time periods. The time duration of the drive pulses (i.e., the duty cycle) depends on the load that is connected to the converter. In contrast, PFM mode operation varies the frequency with which the drive pulses are generated. That is, the pulses have the same duration (i.e., length) but they are either generated more frequently or less frequently. Again, this depends on the load.

Generating pulses, however, wherein a control signal is periodically compared with a reference signal and a drive signal of a given time duration is provided in response to the comparison does not fall either under the rubric of PWM nor under the rubric of PFM. The reference to Bryson, therefore, does not disclose the claimed invention, either explicitly or implicitly.

Bryson's circuit schematic in Fig. 1 is illustrative of his device. The op-amps 16 and 20 are but "signal conditioning amplifiers" in the voltage control signal path and the op-amp 18 is a signal conditioning amplifier in the current controlling signal path. The effectively functional comparator is the amplifier 22 which provides for the PWM control signal into the digital controls 24. Bryson explains the operation very clearly:

> During heavy loading conditions, the controller functions as a current-mode PWM (pulse width modulation) step down regulator. Under light loads, the regulator functions in the PFM (pulse frequency modulation) or pulse skipping mode. The controller senses the load level and switches between the two operating modes automatically, thus optimizing its efficiency under all loading conditions.

Bryson, col. 3, lines 17-24.

As further explained by Bryson, the comparator 22 provides the main PWM control signal for input into the controller 24. The switch to the frequency modulation ("pulse skipping mode") is effected by "[a]dditional comparators (not shown) in the analog control circuit." Col. 3, lines 57-59.

It is respectfully submitted that Bryson does not disclose (i.e., "clearly anticipate") the claimed invention. Bryson does not provide for the claimed periodic comparison, the result of which causes the driver to either issue a drive signal pulse of a given duration or not to issue a drive signal pulse.

The honorable Board is therefore respectfully urged to reverse the final rejection of the Primary Examiner.

Respectfully submitted,

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Claims Appendix:

15. A switching converter, comprising:

a switch including a control terminal, a first load terminal, and a second load terminal;

a rectifier configuration connected to said switch, said rectifier configuration including a plurality of output terminals for providing an output voltage to a load;

a controller configuration for providing a control signal dependent on the output voltage; and

a drive circuit for generating drive pulses, said drive circuit comparing the control signal with a reference signal in periodical time periods, and, in dependence on the comparison, providing a drive pulse of a given duration or no drive pulse;

said drive pulses turning said switch on and off.

16. The switching converter according to claim 15, wherein said drive circuit is configured for generating the plurality of drive pulses with an identical duration and at an identical time interval depending on whether the control signal is greater or less than a reference signal.

17. The switching converter according to claim 15, wherein said controller configuration includes a proportional controller, a proportional-integral controller, or an integral controller.

18. The switching converter according to claim 15, wherein said drive circuit includes a clocked comparator configuration being fed with the control signal, a first reference signal and a clock signal.

19. The switching converter according to claim 18, wherein:

the clock signal has a timing;

said clocked comparator configuration generates the plurality of drive pulses if the control signal is greater than the first reference signal; and

the plurality of drive pulses each have a predetermined time duration and a timing corresponding to the timing of the clock signal.

20. The switching converter according to claim 15, wherein said controller configuration is a digital controller configuration providing a discrete-time control signal.

21. The switching converter according to claim 20, wherein:

said drive circuit includes a digital comparator configuration and a pulse shaping filter connected downstream of said digital comparator configuration; and

said pulse shaping filter has an output for providing the plurality of drive pulses.

22. The switching converter according to claim 15, wherein said controller configuration includes a noise shaping filter being fed with a signal dependent on the output voltage.

23. The switching converter according to claim 15, further comprising:

a level converter having an input being fed with the plurality of drive pulses and an output connected to said control terminal of said switch.

24. The switching converter according to claim 15, wherein said rectifier configuration includes a coil connected in series with said switch.

25. A method for driving a switch in a switching converter having a rectifier configuration connected to the switch, the method which comprises:

generating a control signal dependent on an output voltage provided by the rectifier configuration; and

comparing the control signal with a reference signal in periodical time periods to form a comparision result; and

generating a drive signal with drive pulses and, depending on the comparison result, providing a drive pulse of a given duration or no drive pulse.

26. The method according to claim 25, which comprises:

providing the control signal with a signal component formed by integrating a differential signal made from a signal proportional to the output voltage and a reference signal.

27. The method according to claim 25, which comprises:

providing the control signal with a signal component proportional to the output voltage.

28. The method as according to claim 25, which comprises forming the drive pulses with a timing of a clock signal depending on whether the control signal is greater or less than a reference value.

Evidence Appendix:

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or any other evidence has been entered by the Examiner and relied upon by appellant in the appeal.

Related Proceedings Appendix:

No prior or pending appeals, interferences or judicial proceedings are in existence which may be related to, directly affect or be directly affected by or have a bearing on the Board's decision in this appeal. Accordingly, no copies of decisions rendered by a court or the Board are available.